

## SCAN DRIVING CIRCUIT FOR USE IN PLANAR DISPLAY

### FIELD OF THE INVENTION

**[0001]** The present invention relates to a scan driving circuit, and more particularly to a scan driving circuit for use in a planar display.

### BACKGROUND OF THE INVENTION

**[0002]** With the increasing development of manufacturing technology, the semiconductor materials used for fabricating TFTLCDs (Thin film transistor-Liquid crystal displays) are generally low-temperature polysilicon (LTPS) in place of traditional amorphous silicon. The LTPS-TFT has higher electronic mobility than the TFT made of amorphous silicon. A typical liquid crystal display principally comprises a scan driving circuit and an active matrix. Conventionally, the active matrix is disposed on the display panel, and the scan driving circuit for driving the active matrix is arranged outside the display panel. Whereas, the scan driving circuit and the active matrix are integrated into the display panel in current liquid crystal displays. The common processes for fabricating integrated circuits comprise NMOS, CMOS and PMOS processes. Since the PMOS process involves in least masking numbers and least manufacturing steps among these processes, the PMOS process is widely employed to fabricate scan driving circuits and active matrices of display panels, especially large-size display panels.

**[0003]** Since the sizes of panel displays are growing larger and larger, single scan driving circuit could not catch up with the requirement on driving capability. Therefore, a bilateral scan driving circuit is developed for a purpose of enhancing driving capability. Fig. 1 is a schematic circuit block diagram illustrating the configuration of a conventional bilateral scan driving circuit for

use in a LCD panel. The bilateral scan driving circuit comprises two vertical scan driving circuits 11 disposed on both sides of the active matrix 10. Each of the vertical scan driving circuits 11 comprises a plurality of sub-circuits, e.g. DC1, DC2 and DC3 as shown. Each sub-circuit comprises a shift register, e.g. A1, A2 and A3 as shown, a buffer circuit, e.g. B1, B2 and B3 as shown, and an electro-static discharge (ESD) protection circuit, e.g. C1, C2 and C3 as shown. In spite three sub-circuits are illustrated to be included in each vertical scan driving circuit are shown in the drawing, more than three sub-circuits can also be included in a similar manner. In response to a clock signal, each shift register generates a driving signal. For a purpose of increasing driving power, the driving signal is then amplified by the buffer circuit downstream of the shift register so as to turn on the thin film transistors of the same row. The scan lines are successively driven by the vertical scan driving circuits 11 so as to sequentially turn on the thin film transistors row by row. Each ESD protection circuit is used for preventing from ESD damage.

[0004] It is apparent from Fig. 1 that each shift register is controlled by the amplified driving signal from a buffer circuit of the preceding sub-circuit. For example, the shift register A2 is controlled by the amplified driving signal outputted from the buffer circuit B1. Likewise, the shift register A3 is controlled by the amplified driving signal outputted from the buffer circuit B2. Since two adjacent scan lines of the active matrix 10 is possibly shorted, as indicated by the dash line a-b, due to some inherent adverse factors rendered by the manufacturing process, the buffer circuit B2 needs to drive double thin film transistors in the active matrix 10. Therefore, the amplified driving signal from preceding buffer circuit B2 might have insufficient power to drive the shift register A3. Likewise, the buffer circuit B3 also has to drive double thin film

transistors in the active matrix 10. In such circumstance, the successive scan lines could not be effectively driven to maintain normal operation of the display.

## SUMMARY OF THE INVENTION

**[0005]** It is an object of the present invention to provide a driving circuit for driving an active matrix of a display panel to exempt from the adverse effect of the load of the upstream sub-circuit on the driving capability of the downstream sub-circuit.

**[0006]** In accordance with a first aspect of the present invention, there is provided with a scan driving circuit for use in a planar display comprising an active matrix. The scan driving circuit comprises a first sub-circuit and a second sub-circuit. The first sub-circuit receives a driving signal and outputs the driving signal to a first scan line of the active matrix via a first output terminal after a predetermined time delay. The second sub-circuit is electrically connected to the first sub-circuit, receives the driving signal transferred from a second output terminal of the first sub-circuit, and outputs the driving signal to a second scan line of the active matrix after the predetermined time delay. Furthermore, the first sub-circuit comprises a unidirectional conducting device electrically connected between the first output terminal and the second output terminal.

**[0007]** In an embodiment, the first sub-circuit comprises a shift register and a buffer circuit. The shift register receives the driving signal and outputs the driving signal after the predetermined time delay in response to a clock signal. The buffer circuit is electrically connected to the shift register, the active matrix and the second sub-circuit, amplifies power of the driving signal, and outputs the amplified driving signal to the active matrix and the second sub-circuit via the first output terminal and the second output terminal, respectively.

**[0008]** In an embodiment, the first sub-circuit further comprises an electro-static discharge protection circuit electrically connected to the first output terminal of the buffer circuit for protecting the scan driving circuit from electro-static discharge damage.

**[0009]** In an embodiment, the buffer circuit of the first sub-circuit comprises a plurality of NOT gates arranged in series.

**[0010]** In an embodiment, the buffer circuit of the first sub-circuit comprises at least an NOT gate electrically connected between the first output terminal and the second output terminal in series functioning as the unidirectional conducting device.

**[0011]** In an embodiment, the NOT gates is one selected from a group consisting of an NMOS NOT gate, a PMOS NOT gate and a CMOS NOT gate.

**[0012]** In an embodiment, the second sub-circuit comprises a shift register and a buffer circuit. The shift register is electrically connected to the second output terminal of the first sub-circuit, receives the driving signal transferred from the second output terminal of the first sub-circuit, and outputs the driving signal after the predetermined time delay in response to the clock signal. The buffer circuit is electrically connected to the shift register, the active matrix and the second sub-circuit, amplifies power of the driving signal, and outputs the amplified driving signal to the second scan lone of the active matrix via the first output terminal.

**[0013]** In an embodiment, the second sub-circuit further comprises an electro-static discharge protection circuit electrically connected to the first output terminal of the buffer circuit for protecting the scan driving circuit from electro-static discharge damage.

**[0014]** In an embodiment, the buffer circuit of the second sub-circuit comprises a plurality of NOT gates arranged in series. Preferably, the NOT gates is one selected from a group consisting of an NMOS NOT gate, a PMOS NOT gate and a CMOS NOT gate.

**[0015]** In accordance with a first aspect of the present invention, there is provided with a scan driving circuit for driving an active matrix of a planar display. The scan driving circuit comprises a plurality of sub-circuits each in communication with one of scan lines of the active matrix. One of the sub-circuits comprises a signal receiving device, a signal amplifying device, a unidirectional conducting device and a second output terminal. The signal receiving device is used for receiving a driving signal from preceding sub-circuit. The signal amplifying device is used for amplifying power of the driving signal and outputting an amplified driving signal. The unidirectional conducting device is disposed downstream of the signal amplifying device for transferring the amplified driving signal to the one of the scan lines unidirectionally via a first output terminal. The second output terminal is electrically connected to the signal amplifying device and next sub-circuit for transferring the amplified driving signal to the next sub-circuit.

**[0016]** In an embodiment, the signal receiving device is a shift register.

**[0017]** In an embodiment, the driving signal received by the signal receiving device is transferred to the signal amplifying device after a predetermined time delay in response to a clock signal.

**[0018]** In an embodiment, the signal amplifying device and the unidirectional conducting device are included in a buffer circuit.

**[0019]** In an embodiment, the signal amplifying device comprises a plurality of NOT gates arranged in series, and the unidirectional conducting

device comprises at least an NOT gate electrically connected between the first and the second output terminals in series.

**[0020]** In an embodiment, the scan driving circuit further comprises an electro-static discharge protection circuit electrically connected to the one sub-circuit and the one of the scan lines for protecting the scan driving circuit from electro-static discharge damage.

**[0021]** In accordance with a first aspect of the present invention, there is provided with a scan driving circuit for driving an active matrix of a planar display. The scan driving circuit comprises a plurality of sub-circuits each in communication with one of scan lines of the active matrix. One of the sub-circuits comprises a signal receiving device and a buffer circuit. The signal receiving device is used for receiving a driving signal from preceding sub-circuit. The buffer circuit comprises a signal amplifying device for amplifying power of the driving signal to output an amplified driving signal, an output terminal for transferring the amplified driving signal to next sub-circuit, and a unidirectional conducting device for transferring the amplified driving signal to the one of the scan lines unidirectionally.

**[0022]** The above objects and advantages of the present invention will become more readily apparent to those ordinarily skilled in the art after reviewing the following detailed description and accompanying drawings, in which:

#### BRIEF DESCRIPTION OF THE DRAWINGS

**[0023]** Fig. 1 is a schematic circuit block diagram illustrating the configuration of a conventional bilateral scan driving circuit for use in a LCD panel;

[0024] Fig. 2 is a schematic circuit block diagram illustrating the configuration of a scan driving circuit for use in a LCD panel according to a preferred embodiment of the present invention;

[0025] Fig. 3 is a schematic circuit block diagram illustrating the configuration of a buffer circuit; and

[0026] Fig. 4 is a schematic circuit block diagram illustrating the configuration of a PMOS NOT gate.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0027] Please refer to Fig. 2, which illustrates a scan driving circuit for use in a LCD panel according to a preferred embodiment of the present invention. The scan driving circuit is a bilateral scan driving circuit. For neat drawings, however, only the vertical scan driving circuit at one side of the active matrix 20 is shown. The vertical scan driving circuit comprises a plurality of sub-circuits, e.g. DC1, DC2 and DC3 as shown. Each sub-circuit comprises a shift register, e.g. A1, A2 or A3, and a buffer circuit, e.g. B1, B2 or B3, as shown. In spite three sub-circuits are illustrated to be included in each vertical scan driving circuit are shown in the drawing, more than three sub-circuits can also be included in a similar manner. In response to clock signals CKV1~CKV3, each shift register receives and then latches the driving signal from the preceding sub-circuit, and after a predetermined time delay, the driving signal is amplified by the buffer circuit downstream of the shift register. The amplified driving signal is transferred to a corresponding scan line and the next sub-circuit via a first output terminal I1 and a second output terminal I2, respectively. Each sub-circuit of the vertical scan driving circuit further comprises an electro-static discharge (ESD) protection circuit, e.g. C1, C2 or C3 as shown, which is electrically connected to the first output terminal I1 of that sub-circuit for

protecting the scan driving circuit from electro-static discharge damage. The amplified driving signal transmitted from the second output terminal I2 then controls the states of the thin film transistors in next scan line. The scan lines are successively driven by the sub-circuits so as to sequentially turn on the thin film transistors in the active matrix 20 row by row.

**[0028]** For a purpose of avoiding the adverse effect of the load of the upstream sub-circuit on the driving capability of the downstream sub-circuit, for example due to a short circuit, the buffer circuit of each sub-circuit comprises a unidirectional conducting device, e.g. D1, D2 or D3 as shown, which is disposed downstream of the shift register. By means of these unidirectional conducting devices, the amplified driving signal is transferred to one of the scan lines unidirectionally via the first output terminal I1. If two adjacent scan lines of the active matrix 20 are shorted, as indicated by the dash line a-b, the buffer circuit B2 needs to drive double thin film transistors in the active matrix 20. However, the amplified driving signal from preceding buffer circuit B2 can still effectively drive the shift register A3.

**[0029]** Referring to Fig. 3, each buffer circuit comprises a plurality of NOT gates arranged in series. While the upstream ones of the plurality of NOT gates function as an amplifying device for amplifying the driving signal from the shift register, one or more downstream NOT gates, as exemplified in Fig. 4 as a PMOS NOT gate, function as the unidirectional conducting device. The amplified driving signal is provided to drive current scan line via a first output terminal I1 and also transferred to next sub-circuit via a second output terminal I2, respectively. Since NOT gates are used in the unidirectional conducting device, the property of the NOT gate inherently exempts from the dependence of the input driving ability from the output loading. With such configuration, even



when two adjacent scan lines are shorted and thus the driving load of the first output terminal I1 is increased, the driving power transmitted from the second output terminal I2 can still maintain normal.

**[0030]** In addition to PMOS NOT gates shown in Fig. 4, the NOT gates used in the buffers can also be NMOS NOT gates or CMOS NOT gates. Since the PMOS process involves in least masking numbers and least manufacturing steps among these processes, the PMOS process is widely employed to fabricate driving circuits and active matrices of display panels, especially large-size display panels.

**[0031]** From the above description, it is understood that the problems resulted from a short circuit can be effectively reduced by means of the arrangement of the unidirectional conducting device in the circuit of the present invention.

**[0032]** While the invention has been described in terms of what is presently considered to be the most practical and preferred embodiments, it is to be understood that the invention needs not be limited to the disclosed embodiment. On the contrary, it is intended to cover various modifications and similar arrangements included within the spirit and scope of the appended claims which are to be accorded with the broadest interpretation so as to encompass all such modifications and similar structures.